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LECTURE NOTES FROM THE FAA ACADEMY 9020 COURSE "IBM 9020D/E SYSTEMS 7201-02 COMPUTING ELEMENT" (ENHANCED IBM S/360 MODEL 65)

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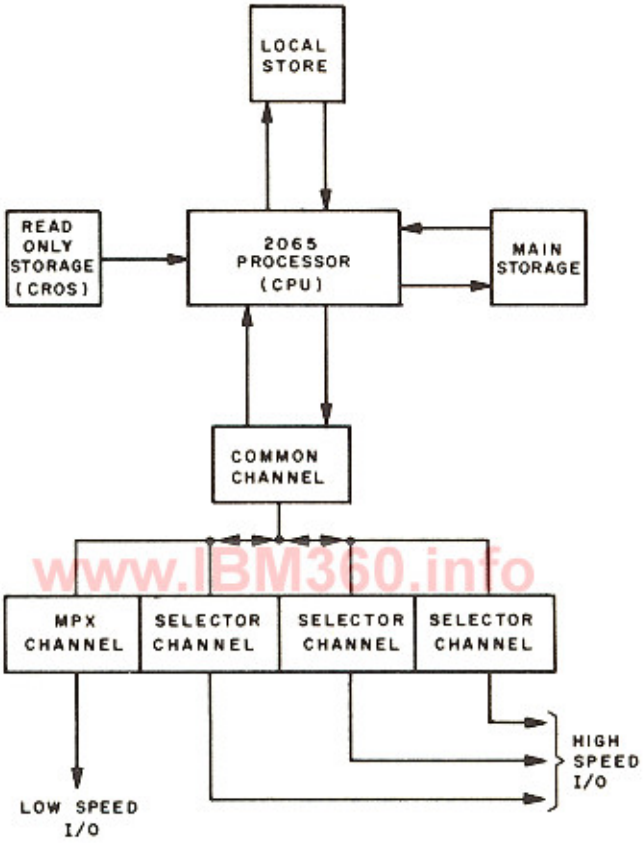

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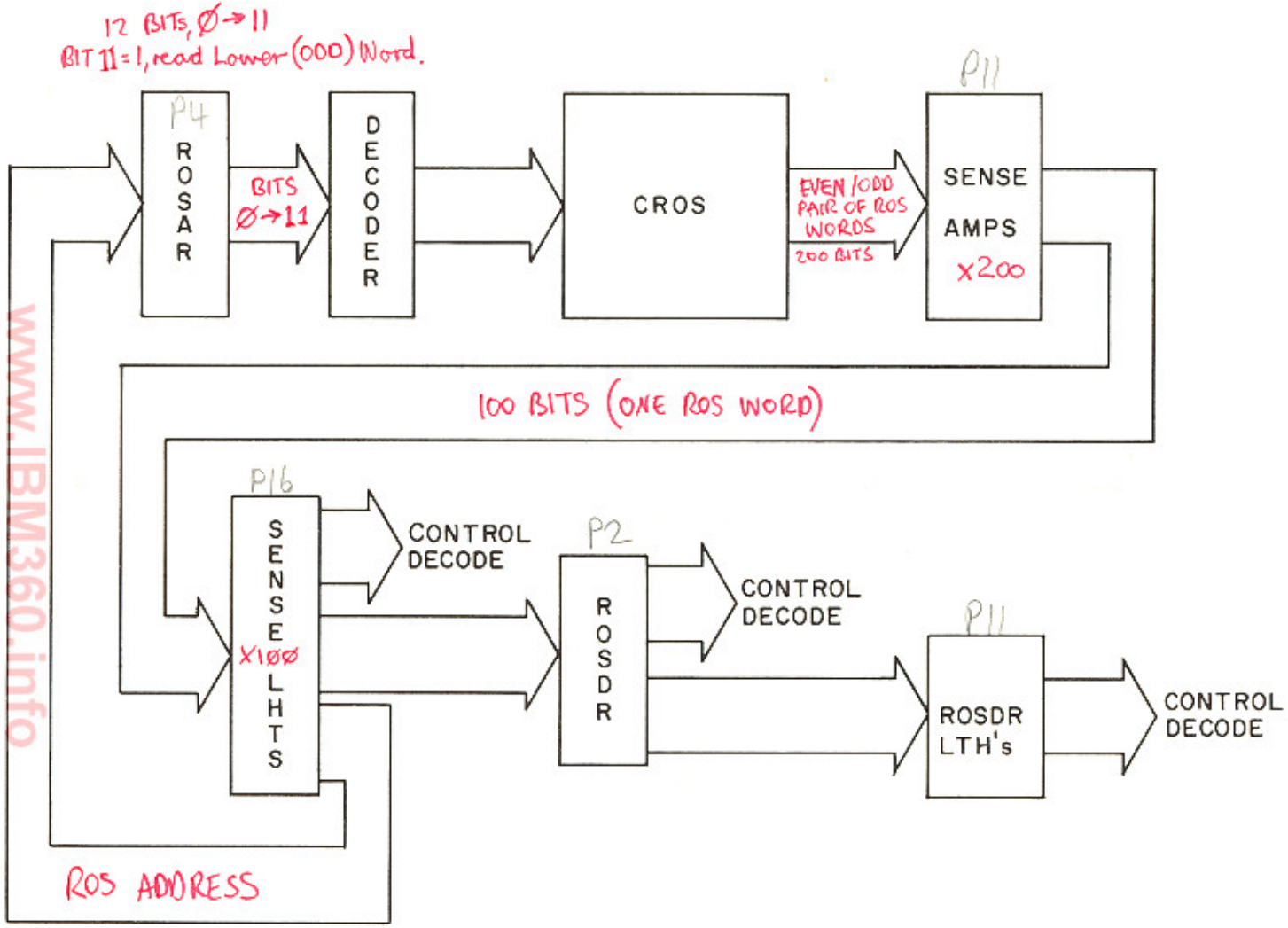
Basic Computer

1-1



CROS "Big Picture"

1-2

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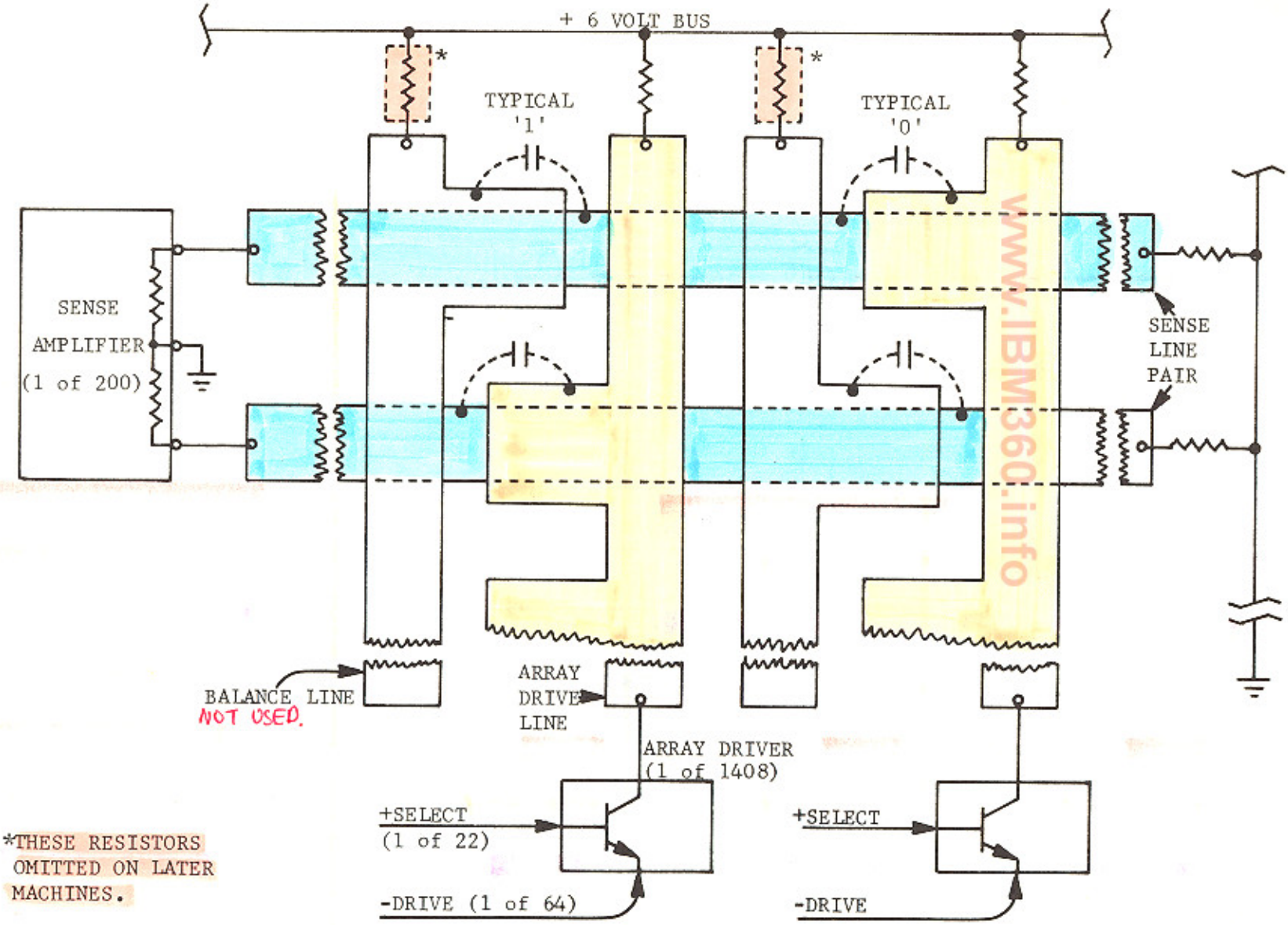

*THESE RESISTORS OMITTED ON LATER MACHINES.

C R O S H A R D W A R E

SEE FETOM P2-10

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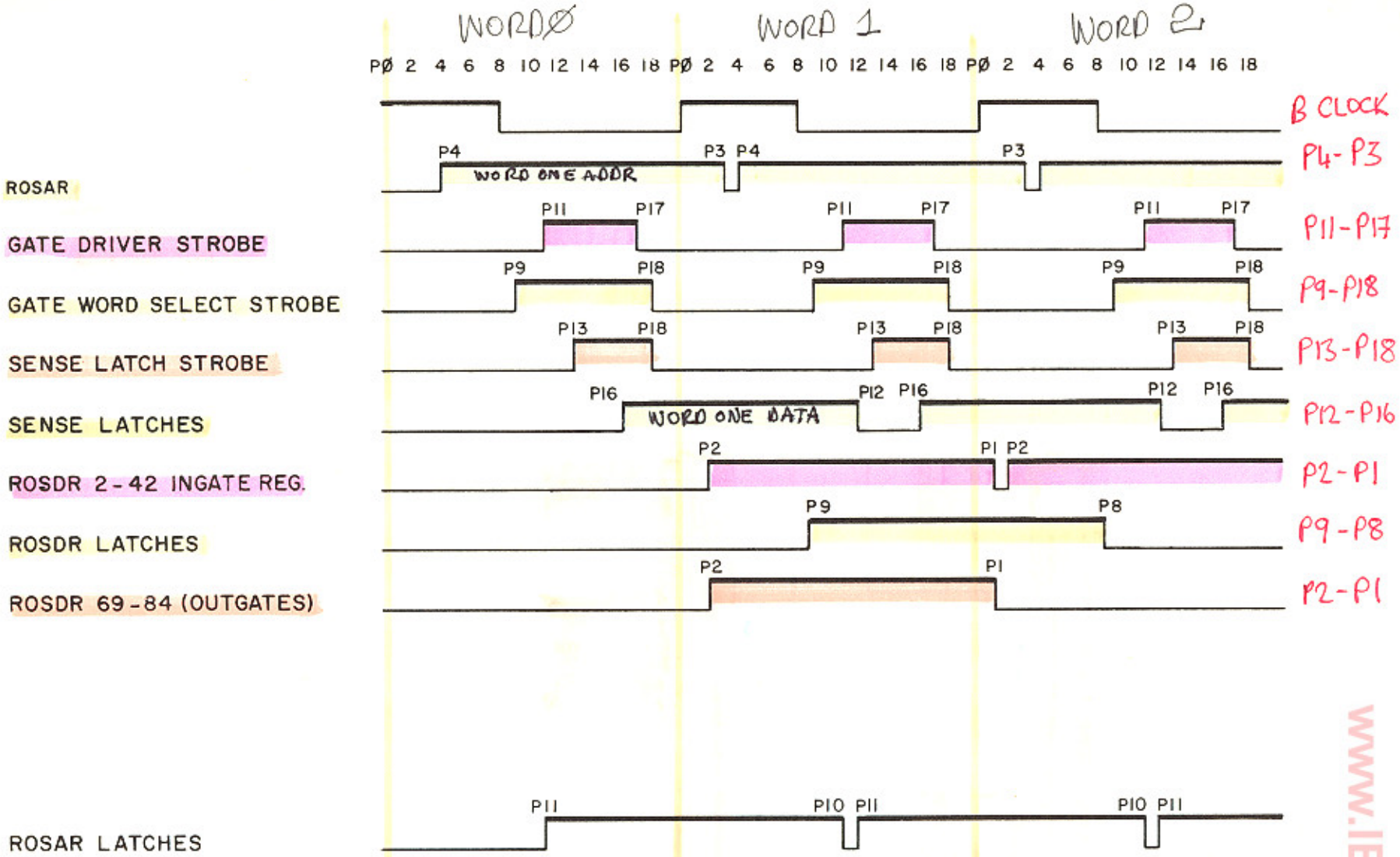

ROS TIMING See FETOM 1-27

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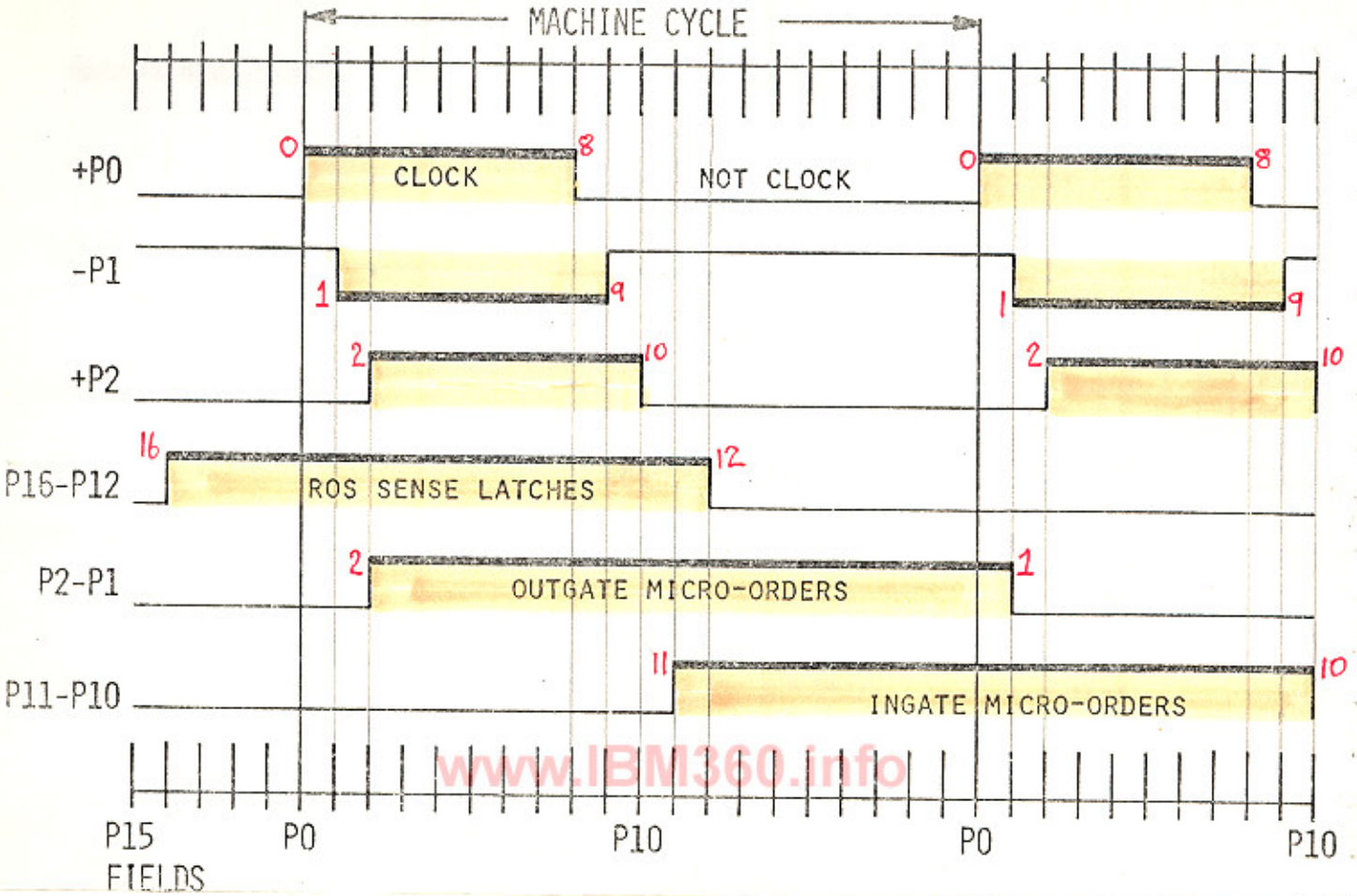

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A. P2-P1 (A7 ONLY)
P11-P10 (ALL OTHERS)

B. P11-P10

C. P2-P1 (C3 ONLY)
P11-P10

D. P2-P1 (D1, D2, D3)
P11-P10 (ALL OTHERS)

E. P2-P1
P11-P10

F. P2-P1
P11-P10

G. P2-P1
P11-P10

H. P2-P1

L. P16-P12

NA. P16-P12

K. P16-P12

J. P16-P12

M. P2-P1

N. P2-P1

P. P2-P1

Q. P2-P1

R. P2-P1

T. P2-P1

U. P2-P1

V. P2-P1

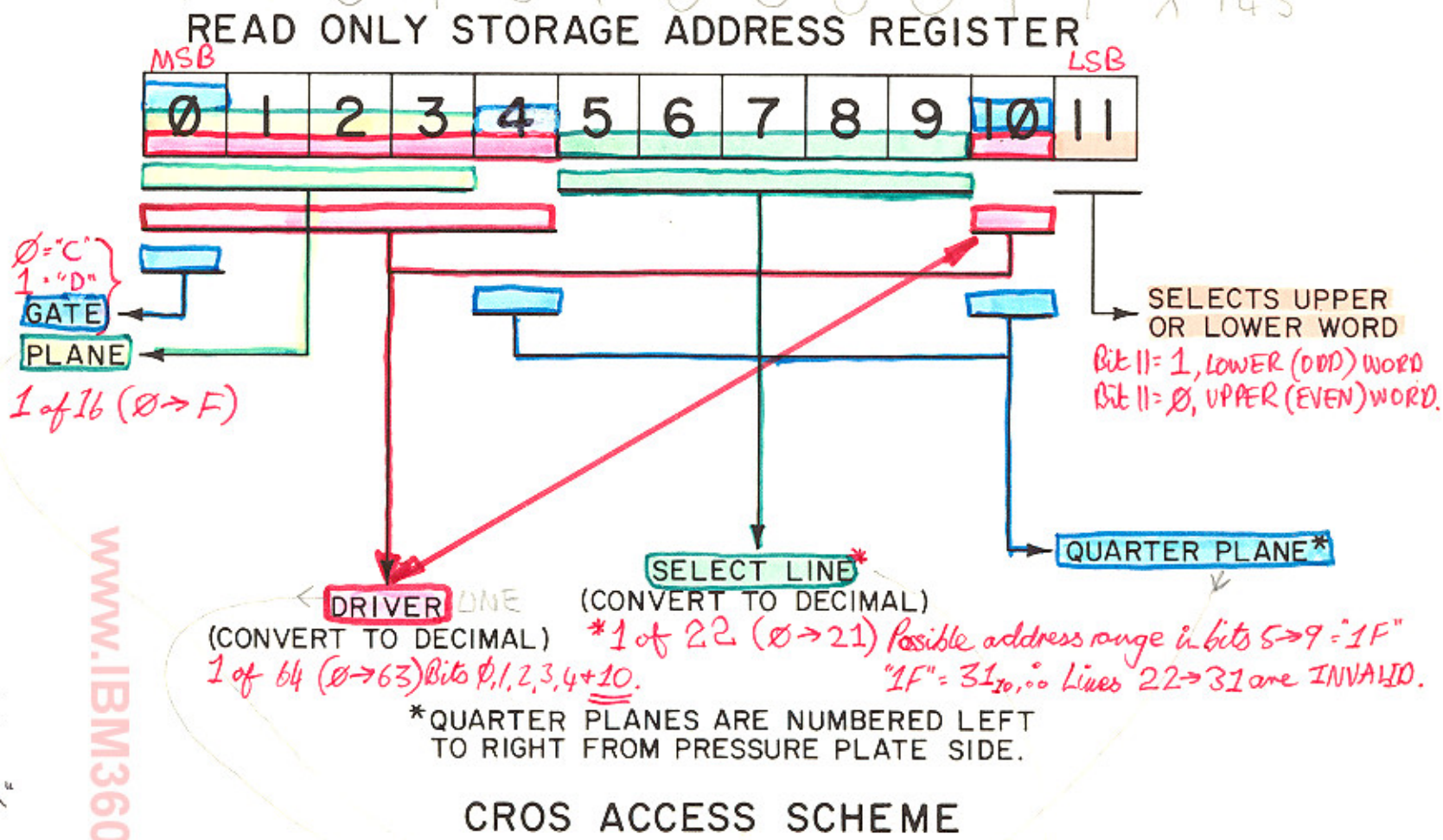
W. P2-P1
P11-P10

ROS FIELD TIMING

SEE FETOM P 1-20

Any ROS address "XD8"→"XFF" is invalid. Any ROS address above "FD7" is invalid.

1 0 0 1 0 1 0 0 0 0 1 1 = X"943"



*QUARTER PLANES ARE NUMBERED LEFT TO RIGHT FROM PRESSURE PLATE SIDE.

EG:- ADDR. "FAA"

GATE - 1 = "D"
PLANE - F = "15"
DRIVER - 3F = "63"
SEL. LINE - "A" = 1Ø
½ PLANE - "3"
WORD - Ø = "UPPER"

CROS ACCESS SCHEME

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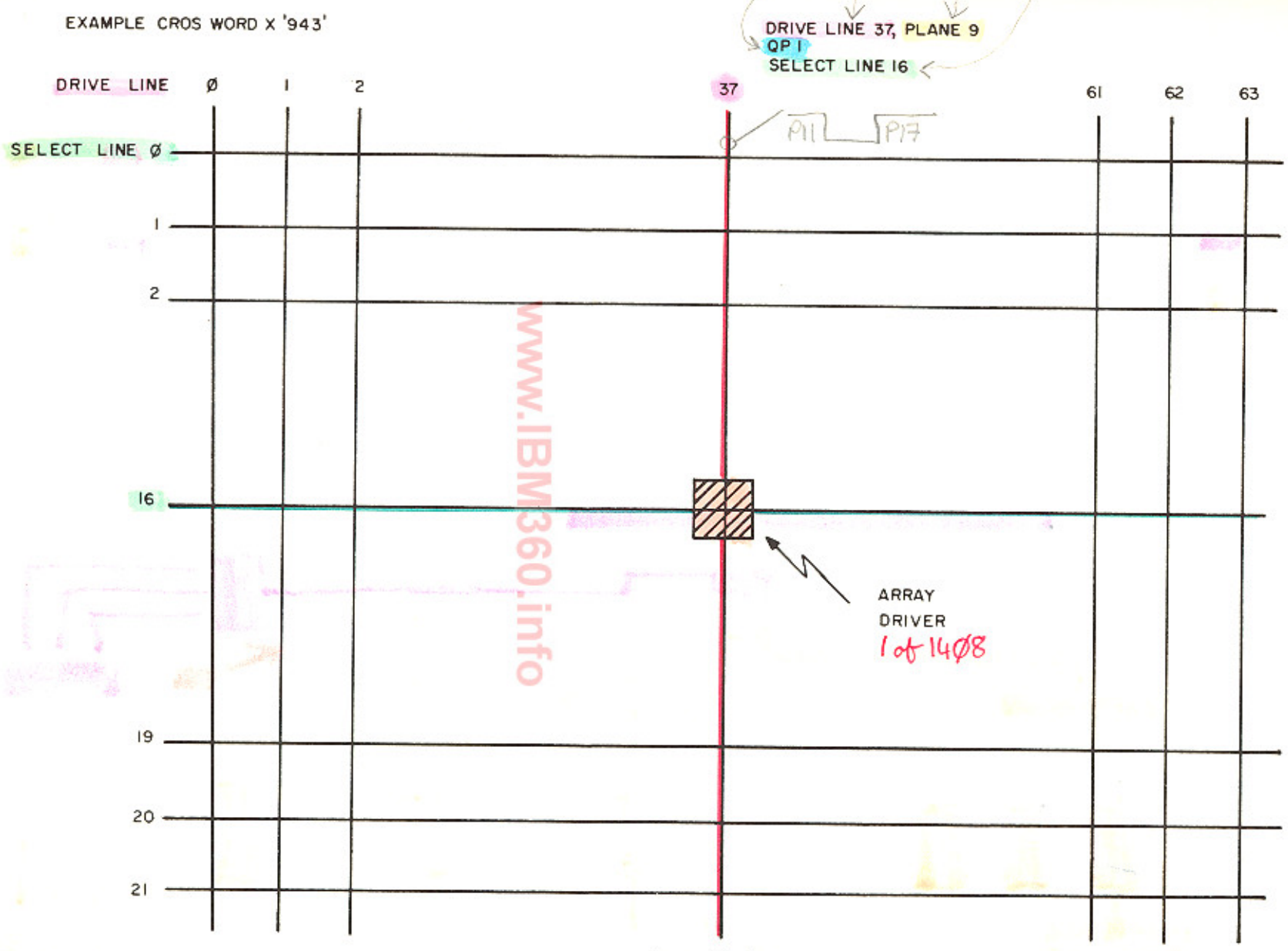
EXAMPLE CROS WORD X '943'



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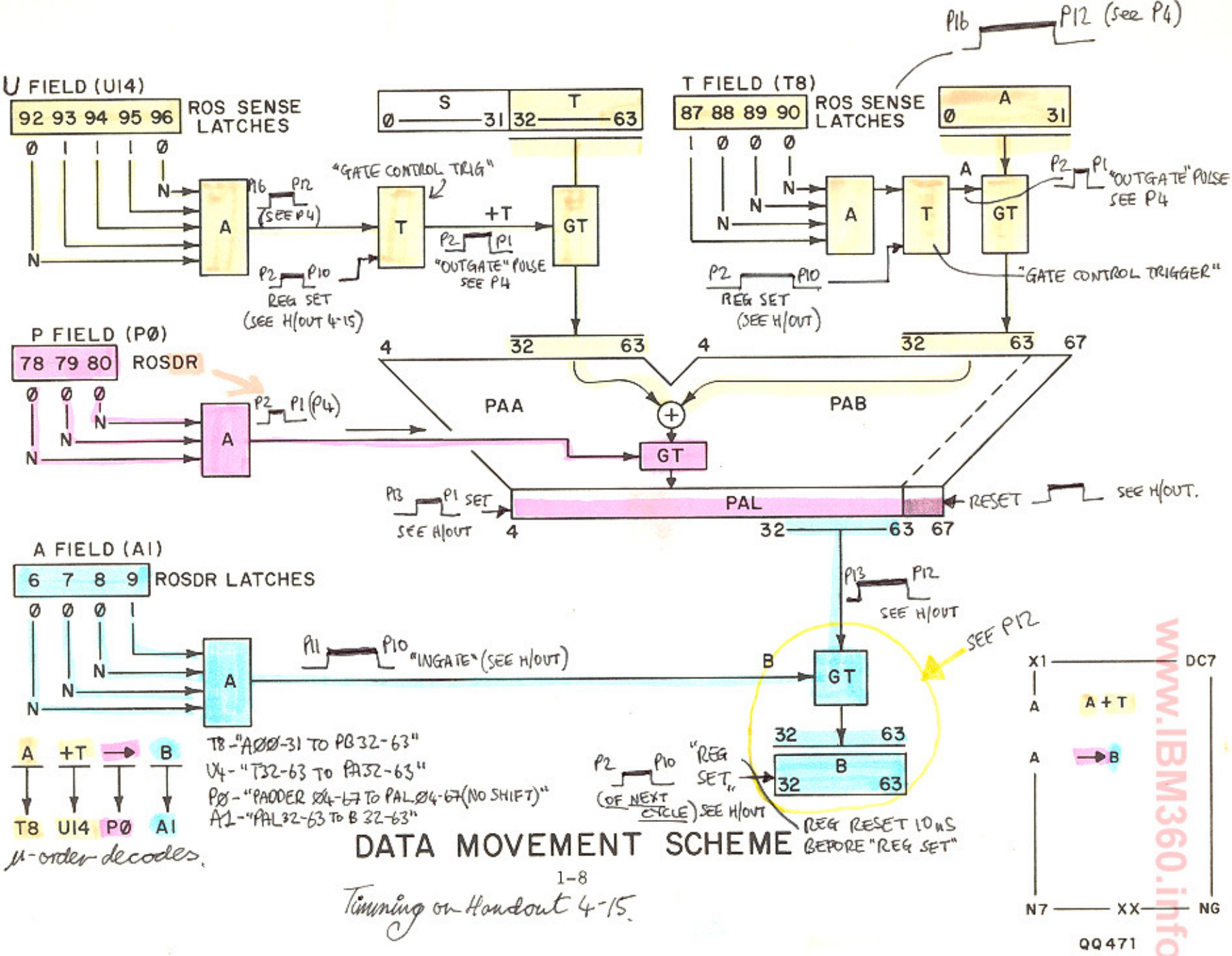
Array Driver



DATA MOVEMENT SCHEME

1-8

Timing on Handout 4-15.

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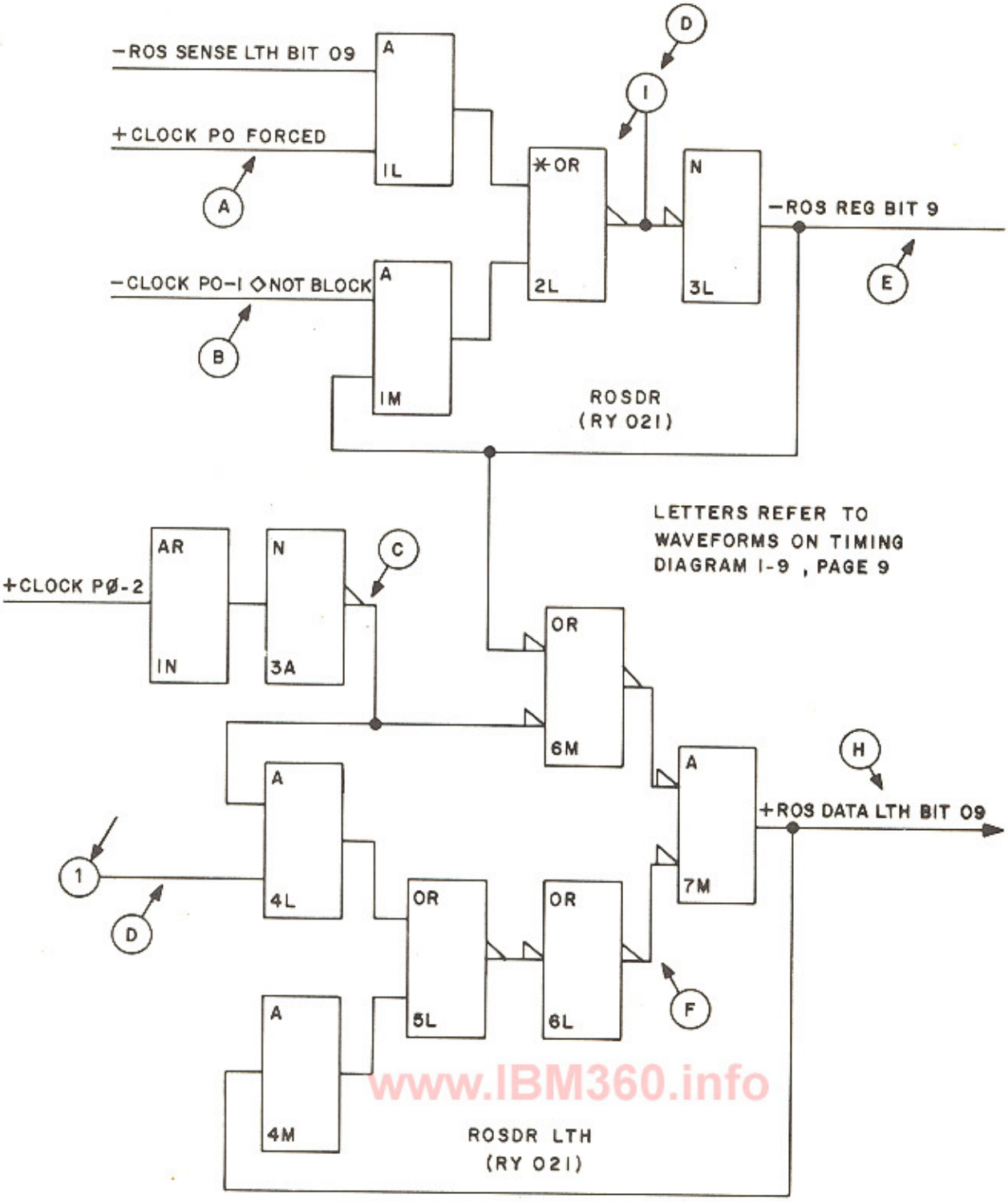

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DECODE A1 MICRO-ORDER BIT 9
(GATE PAL TO B REG)

ROS WORD	BIT W	X	Y	Z
ASSUME ROS SENSE LTH BIT 9	Ø -	1 -	Ø -	Ø

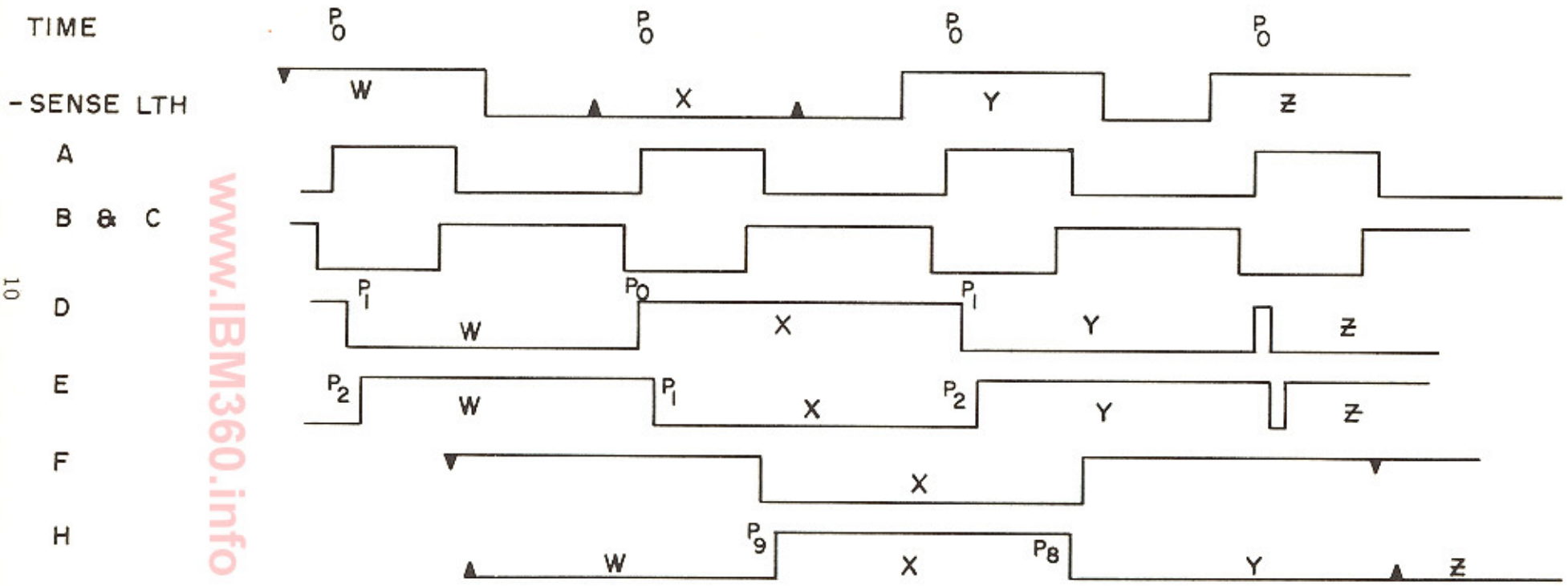

FIG 1-9
LOCATIONS

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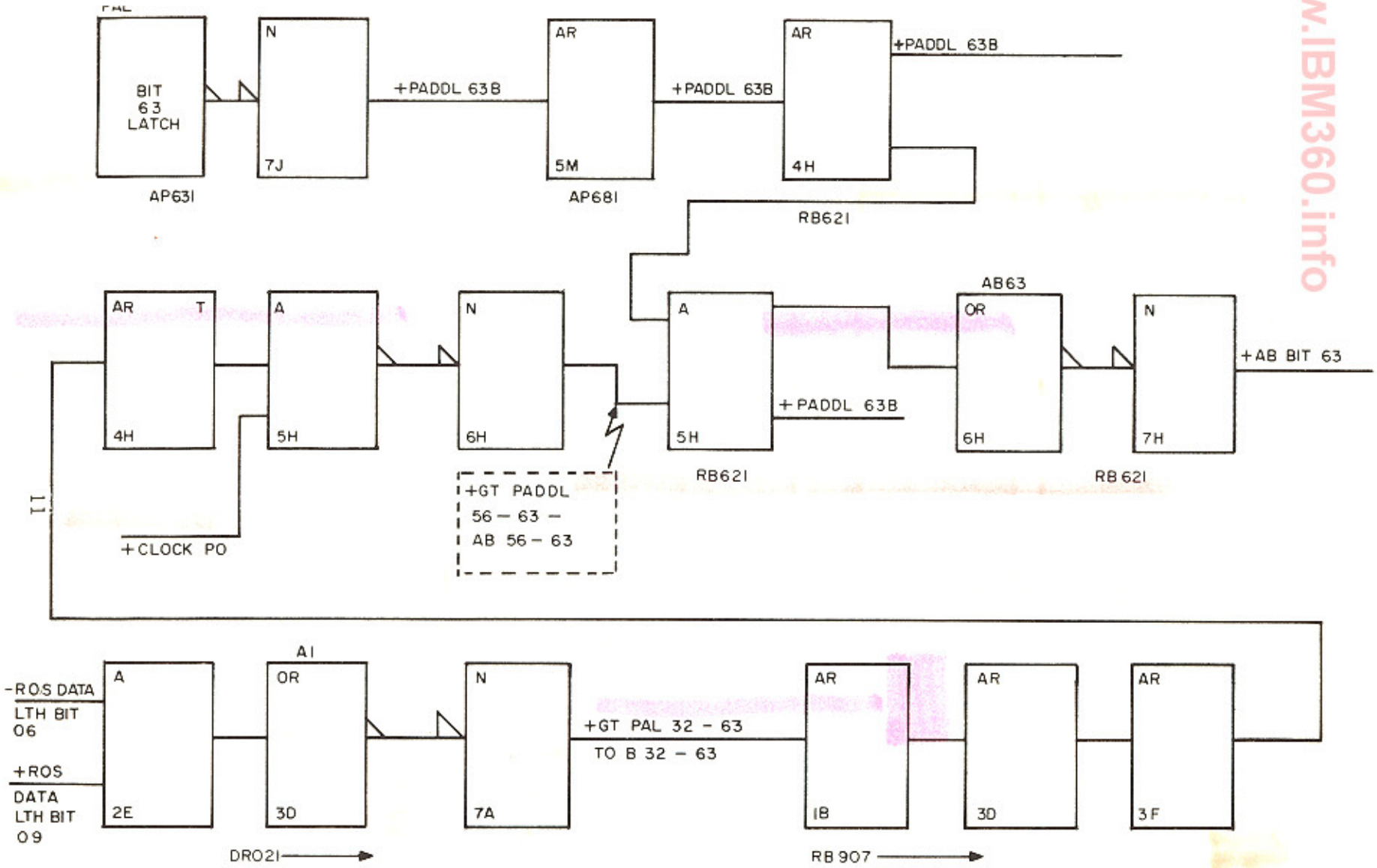
ROSDR - ROSDR LTH TIMING



PAL to B Data Movement

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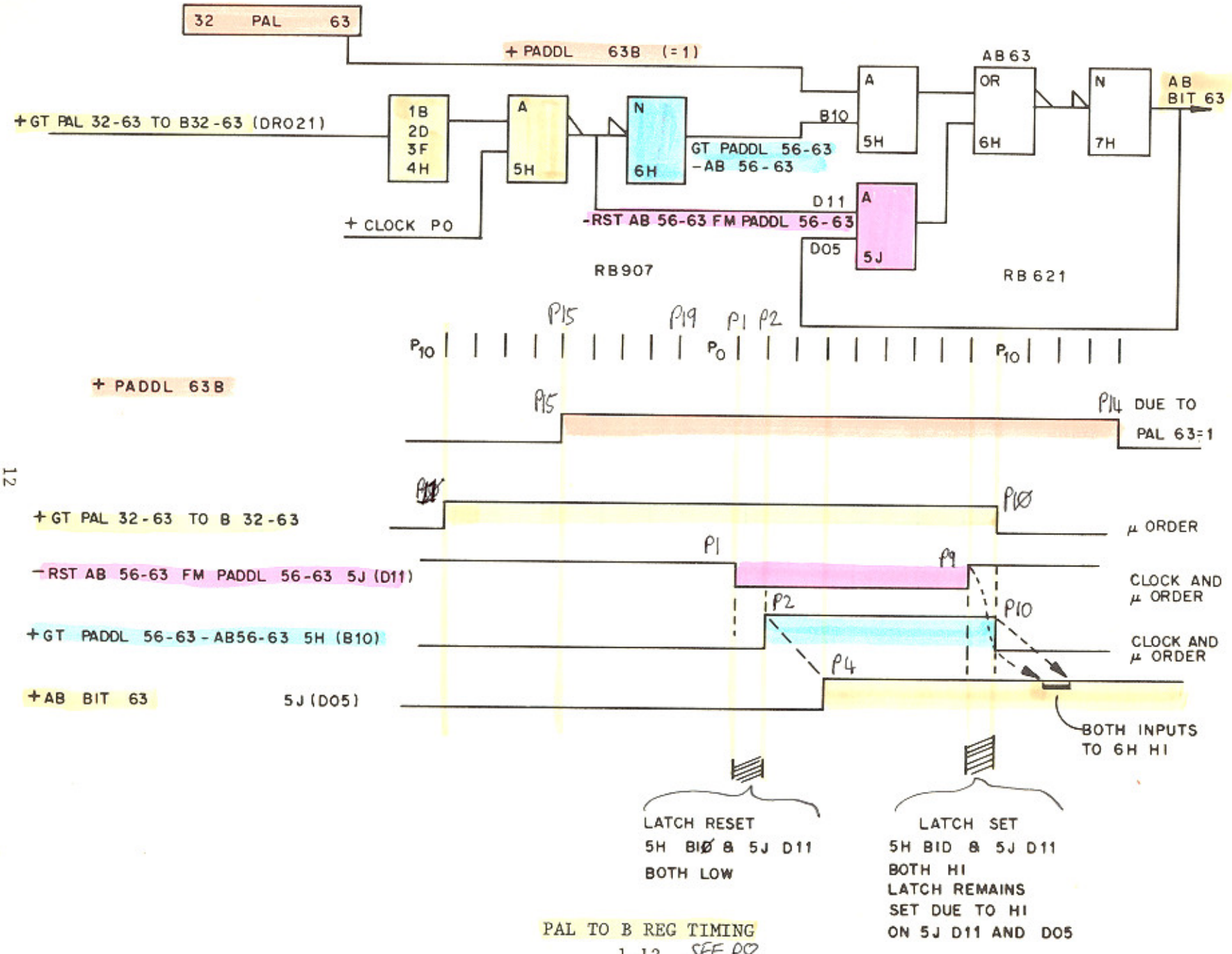

PAL TO B REG TIMING
1-12 SEE P8

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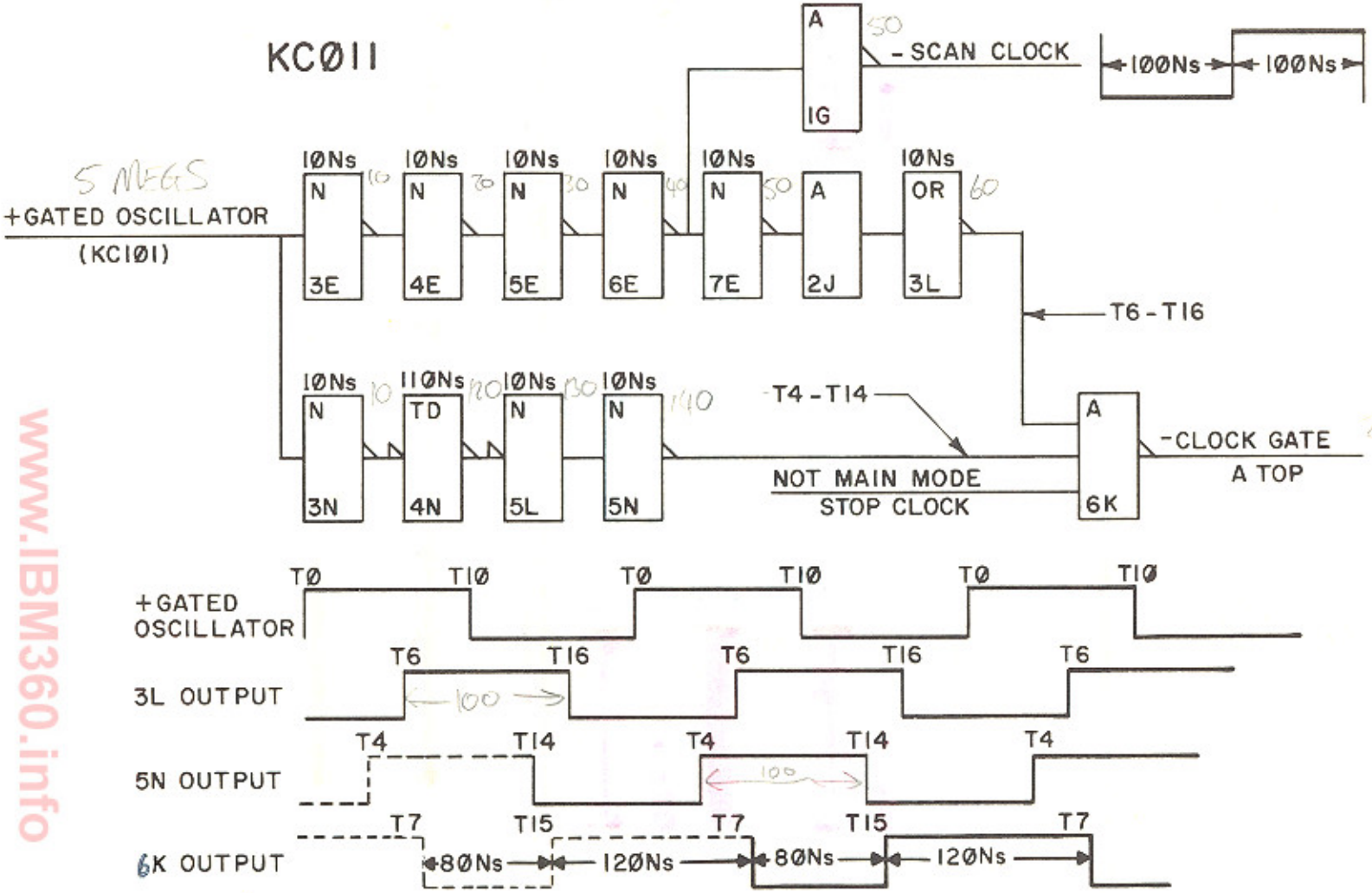

CLOCK FORMATION

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MACHINE - LANGUAGE PROGRAM

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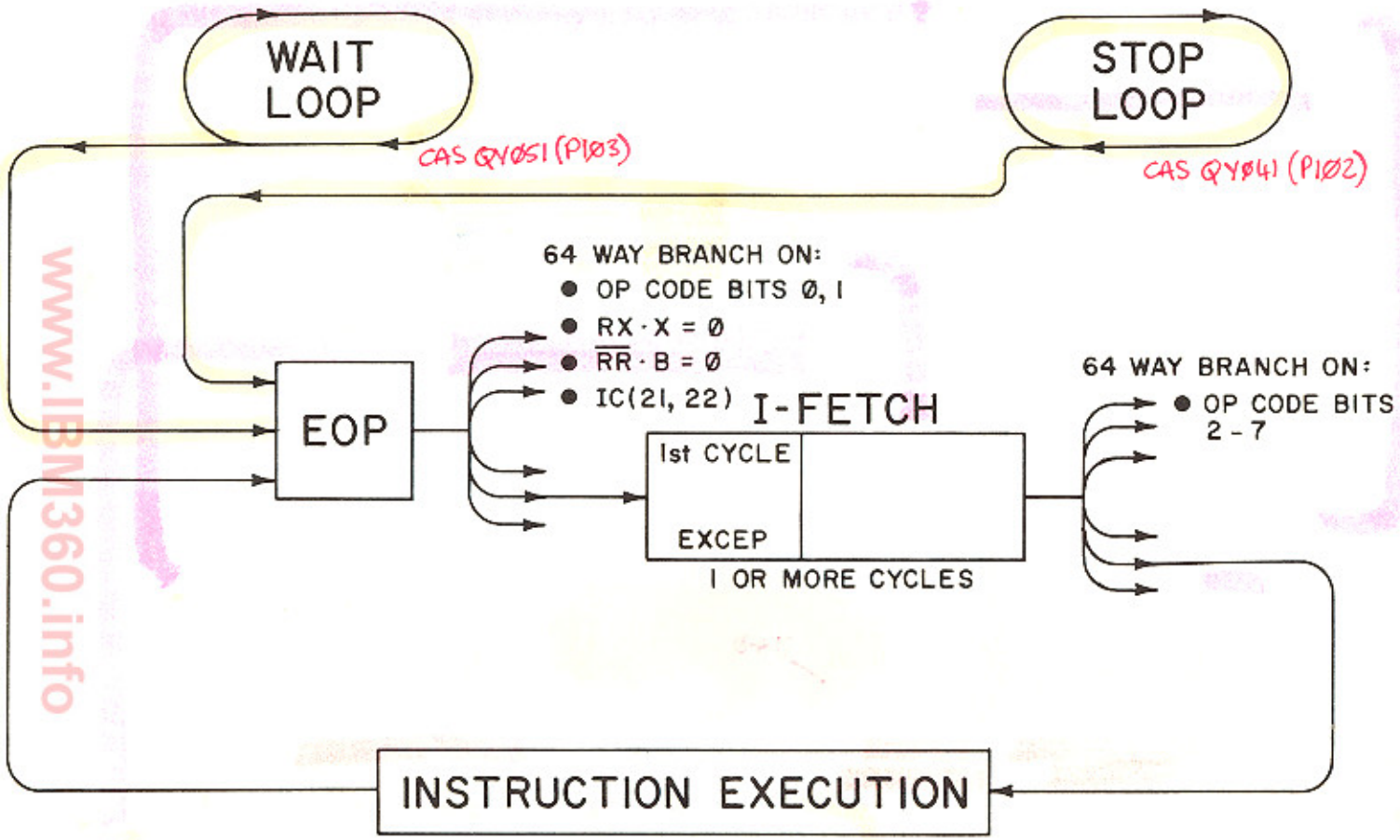
Storage Location	Data & Explanation of Data	
IPSW LOC	IPSW	INST. ADR.
000000	X X X X X X X X	X X 0 0 1 0 0 0
001000	(BALR) R1 R2 0 5 6 0	(LM) R1 R3 9 8 0 5	B D I S (ST) R1 X 6 0 1 2 5 0 4 5
001008	B D I S 6 0 2 A	(AP) L1 L2 F A 2 1	B1 D I S B2 D I S 6 0 2 B 6 0 2 E
001010	(SCON) R1 R2 0 1 2 4	(SATR) R1 R2 0 D 0 1	Reg 0 (ATR 1 Msk) FOR SATR 4 3 1 2 0 0 0 0
001018	Reg 1(ATR 2, Select) FOR SATR 0 0 0 0 0 0 4 2	Reg 2 (Config. Msk) FOR SCON A 0 F 0 0 4 0 2
001020	Reg 3 (Config. Msk) FOR SCON 0 0 0 0 0 0 0 0	Reg 4 (R1 for ST) FOR SCON (Select Msk) 0 0 F 0 0 4 0 2
001028	Reg 5 (X for ST) 0 0 0 0 0 0 0 8	AP Op 1 L1 FIELD - 3 BYTES X X 4 5 6 7 8 C SIGN
001030	AP Op 2 L2 FIELDS - 2 BYTES 7 8 9 C X X X X SIGN	Stor Wd for Reg 4 (ST) X X X X X X X X



MICROPROGRAM "BIG PICTURE"

2-1

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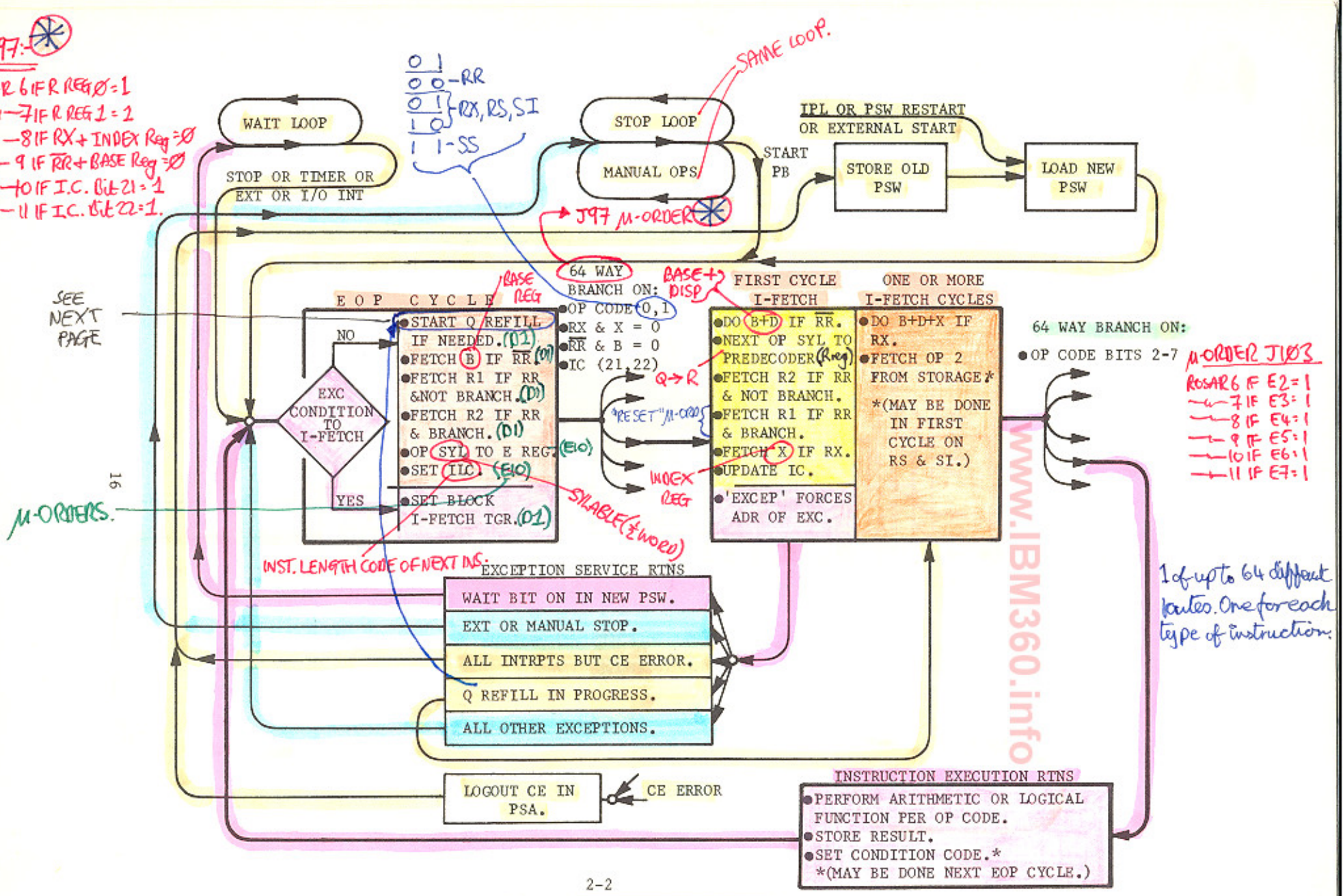

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2-2

9020 D CE MICRO-PROGRAM "BIG PICTURE"

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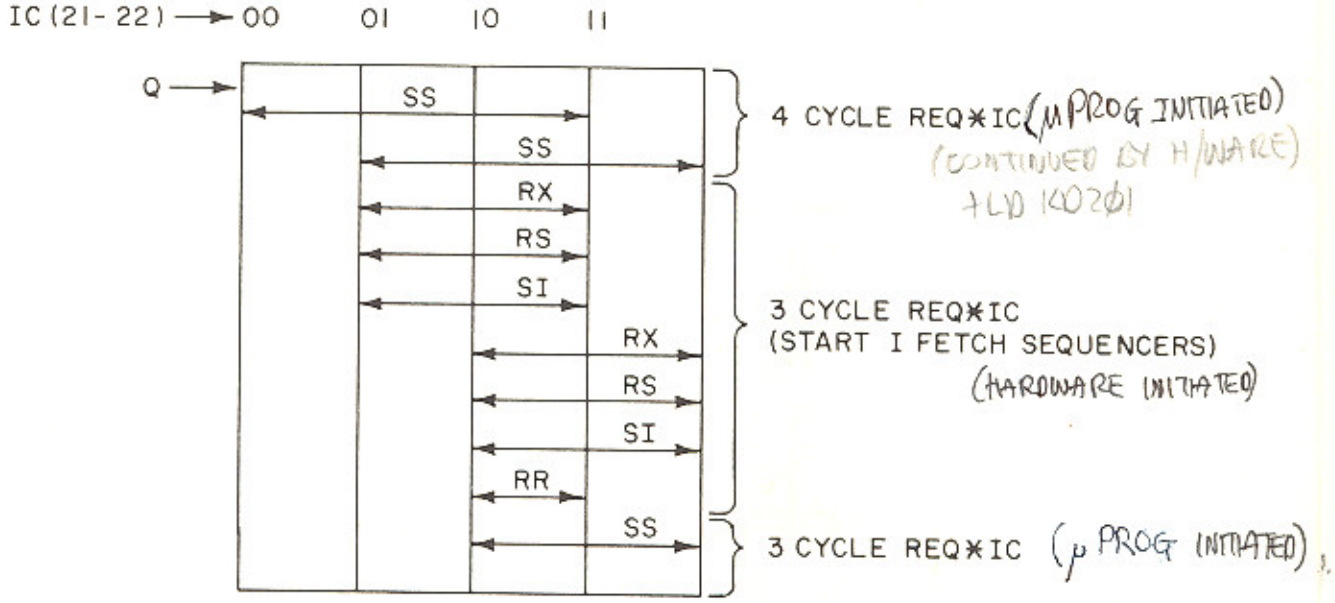
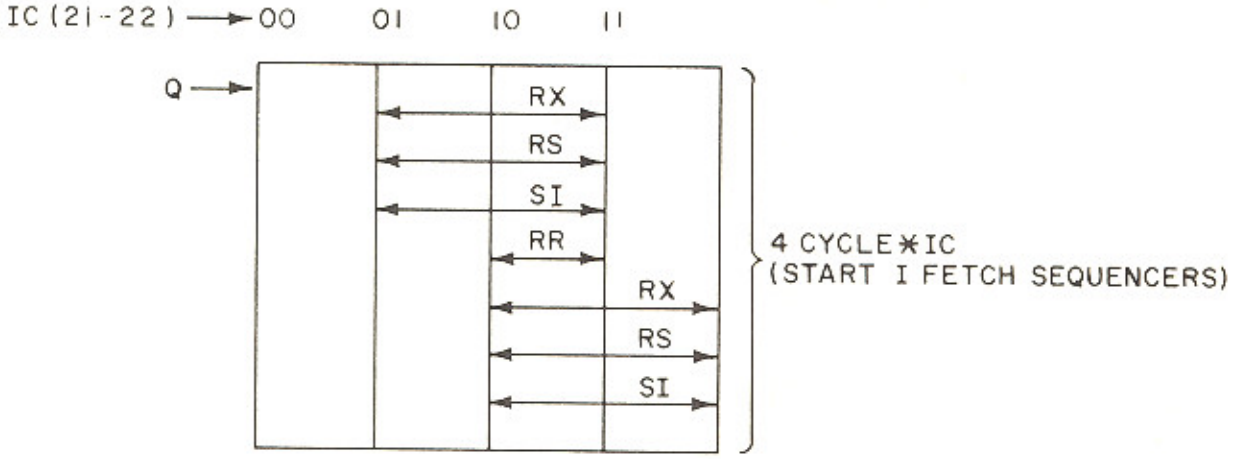
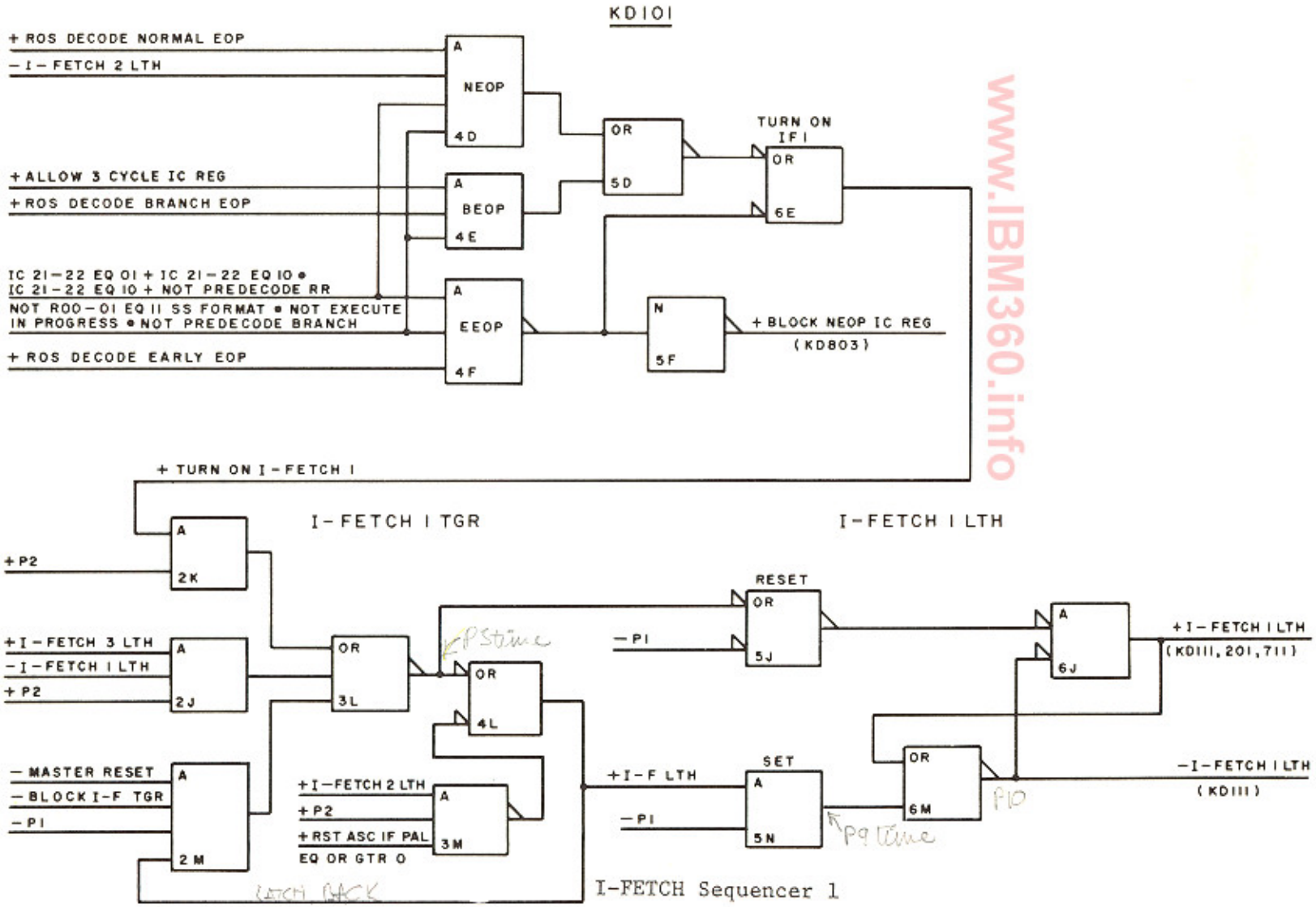
INSTRUCTION REQUEST DURING NEOP OR BEOP
(NOT BRANCH INSTRUCTIONS OR EXECUTE NOT
IN PROGRESS) REF: FEMDM 5-2, 5-30



INSTRUCTION REQUEST DURING EEOP
(NOT BRANCH INSTRUCTIONS OR EXECUTE
NOT IN PROGRESS) REF: FEMDN 5-3, 5-30



Instruction Request During NEOP and BEOP



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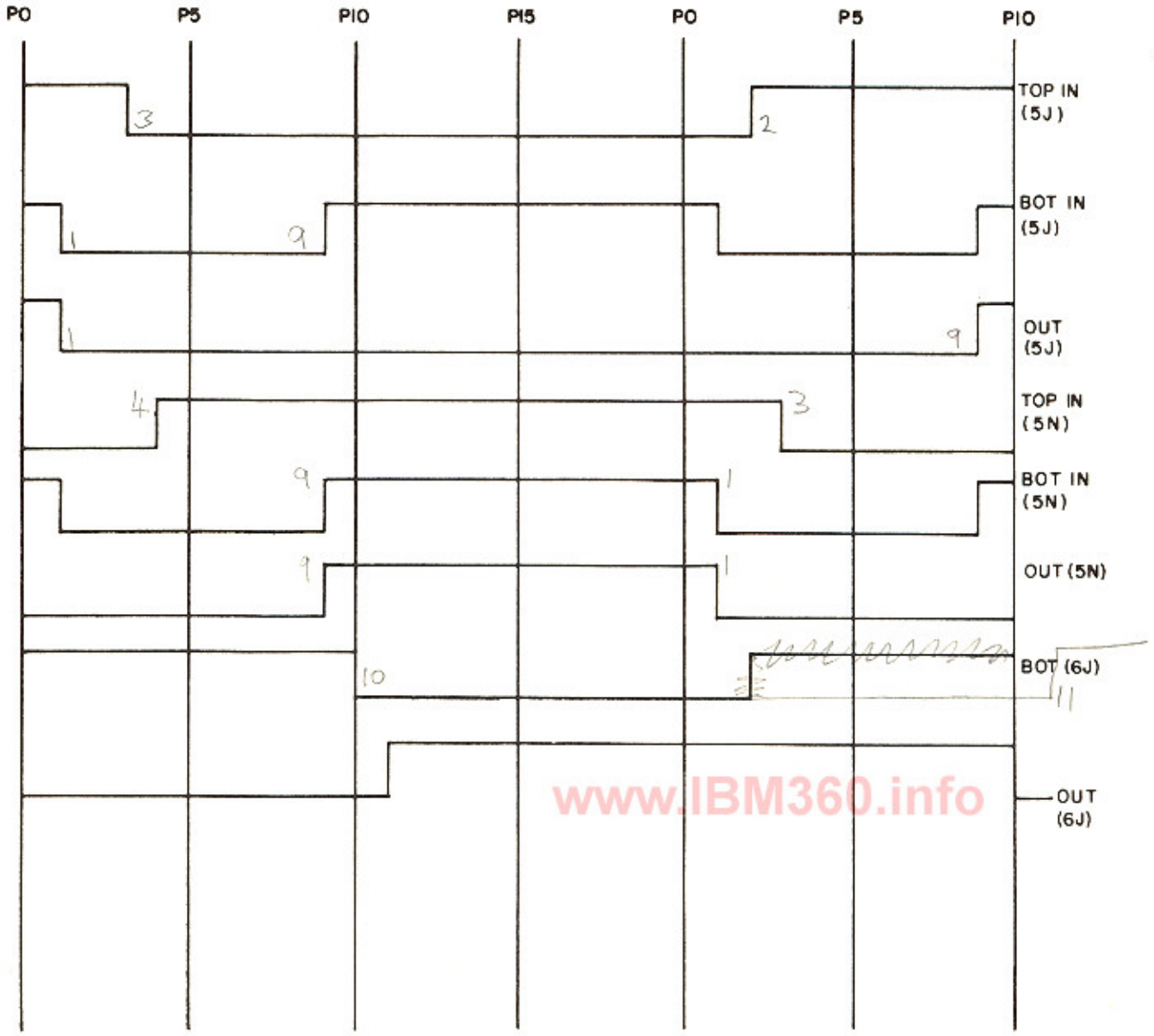

I-FETCH Sequencer 1 Timing

2-5

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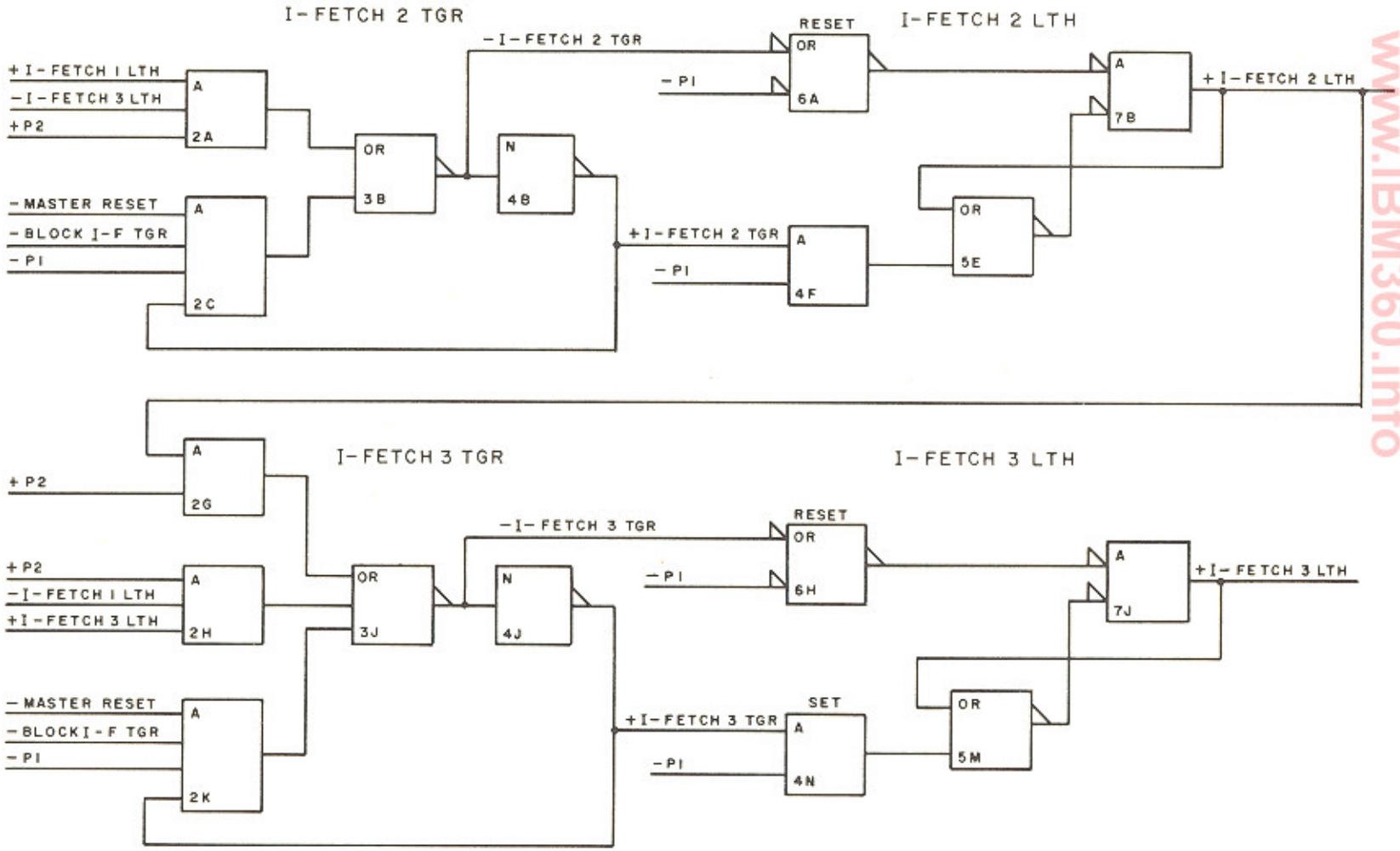

I-Fetch Sequencers 2 and 3

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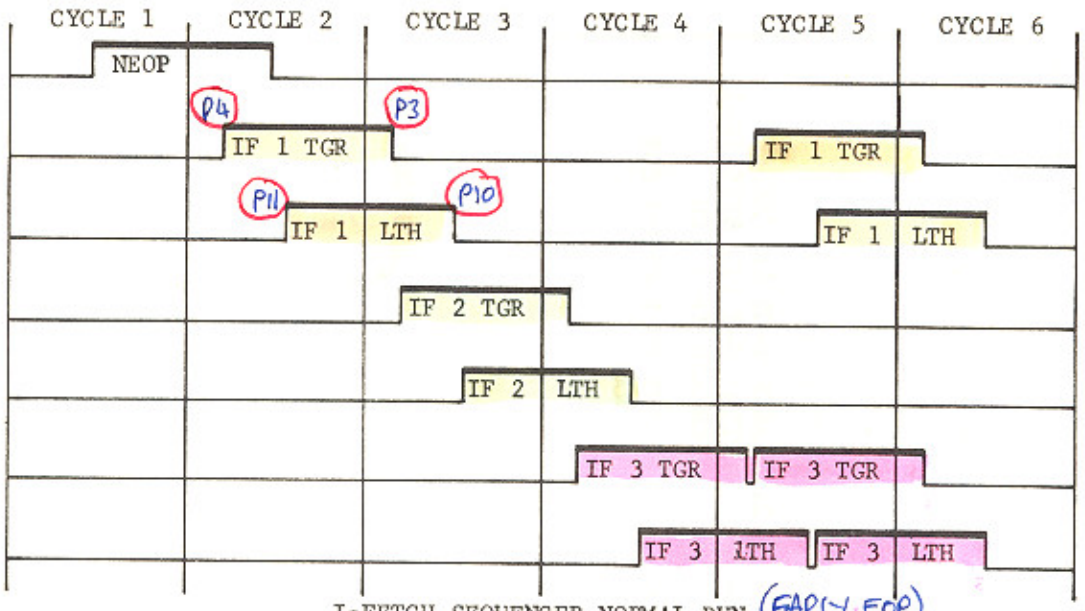
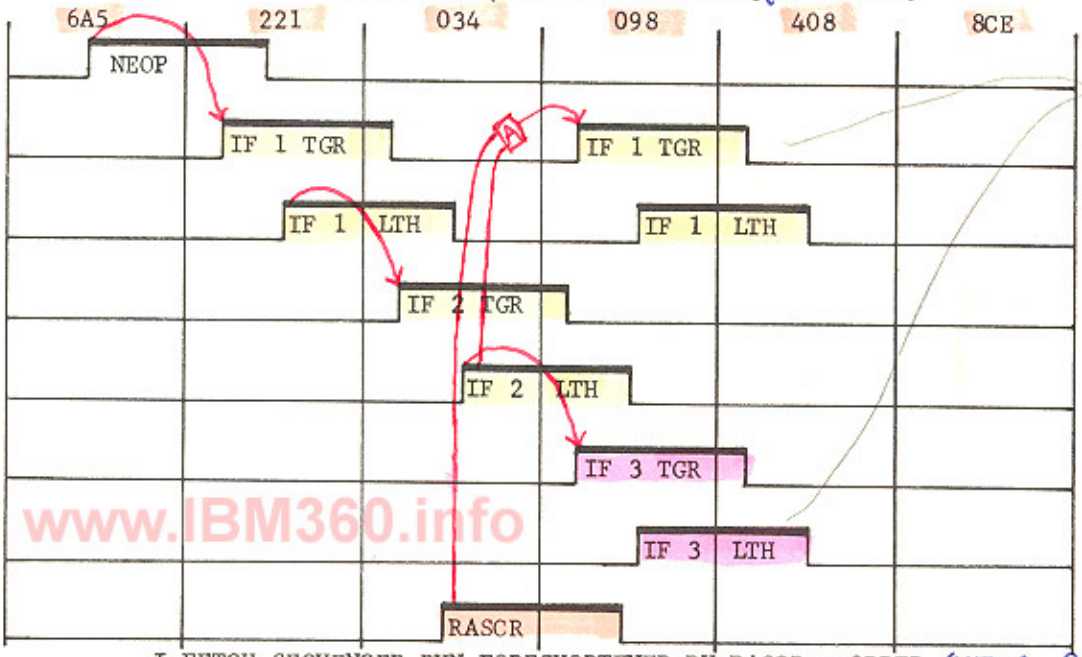


I-FETCH SEQUENCER NORMAL RUN. (EARLY EOP)



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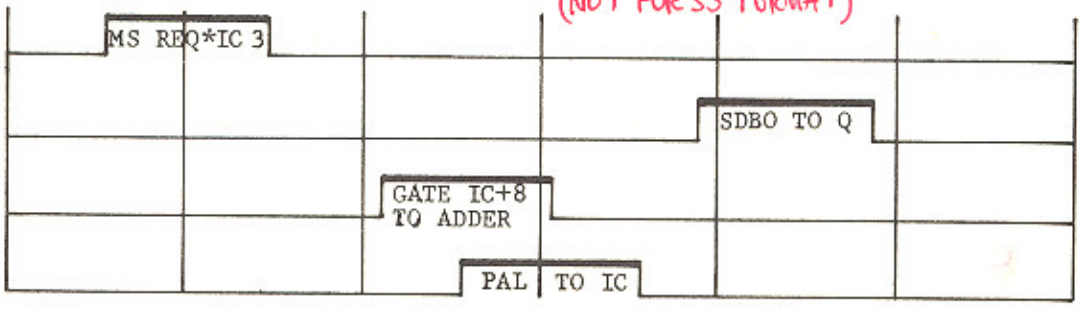
I-FETCH SEQUENCER RUN FORESHORTENED BY RASCR μ-ORDER. (NEOP+ BEOP)
(NOT FOR SS FORMAT)



2-7 See next page. + DE.C.Ø2 P93

I-FETCH

BY HARDWARE

6A5 (QE041) — NEOP — REQ

221 (QT005) — EXCEP — CYC 1

034 (QT041) — REQ — RASCR — CYC 2

P18 1. HARDWARE DETECTS Q REFILL PRIORITY.

P18 2. ISSUE 3-CYCLE REQUEST PER IC.

P18 3. START I-FETCH SEQUENCERS. — DE-C-Ø2 P93

P23 4. SET UP EXCEPTIONAL CONDITION TO I-FETCH.

1. BLOCK μ-ORDER E(02-07)→ROA.

2. EXCEP μ-ORDER FORCES ROSAR TO P23 034.

P27 1. WHEN IF-1 LTH SETS, GATE IC TO PAB, AND SET PAA 60. — INCREASES IC BY 8

P27 2. WHEN IF-2 LTH SETS, GATE PAL (40-63) TO IC.

P18 3. RASCR μ-ORDER "ANDED" WITH IF-2 LTH SETS IF-1 TGR AND IF-1 LTH.

μ-PROG { 4. ISSUE MS REQ*D-3 FOR OPERAND.

5. E(02-07)→ROA.

098 (QK011) — CYC 1 — CYC 3

408 (QK011) — CYC 2

8CE (QK011) — CYC 3

P24 1. IF-3 LTH "ANDED" WITH IF-1 LTH GATES SDBO TO Q. — ~~INSTR.~~ D/WORD COMES FROM S.E.

P25 2. ALSO GATES SDBO (00-15) TO R IF IC(21-22) = 00.

1. MS 1→T GATES SDBO (32-63) TO T.

OPERAND

Q REFILL EXCEPTIONAL CONDITION (NEOP)

Flow Chart in DE-C-Ø2 Page 111.

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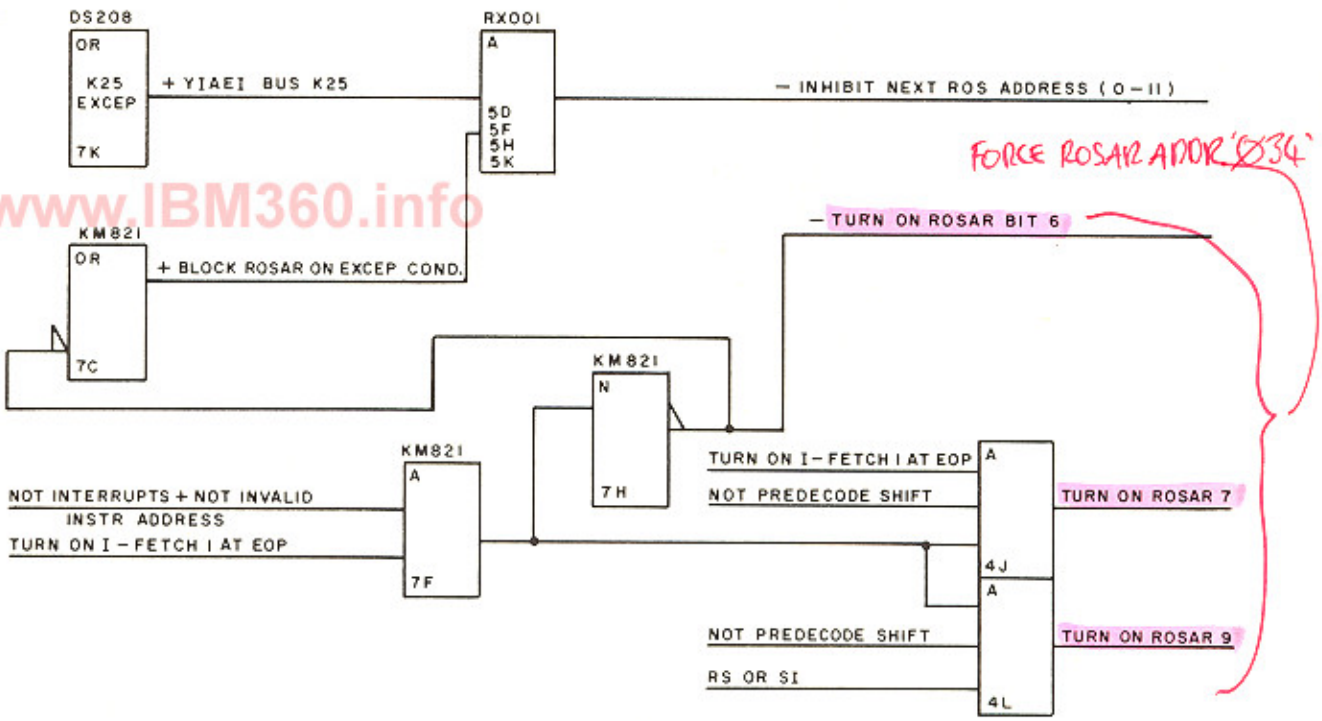

Exception μ-Order For "Q" Refill Priority (ROS Ø34) (RS-SI FORMAT)

2-9

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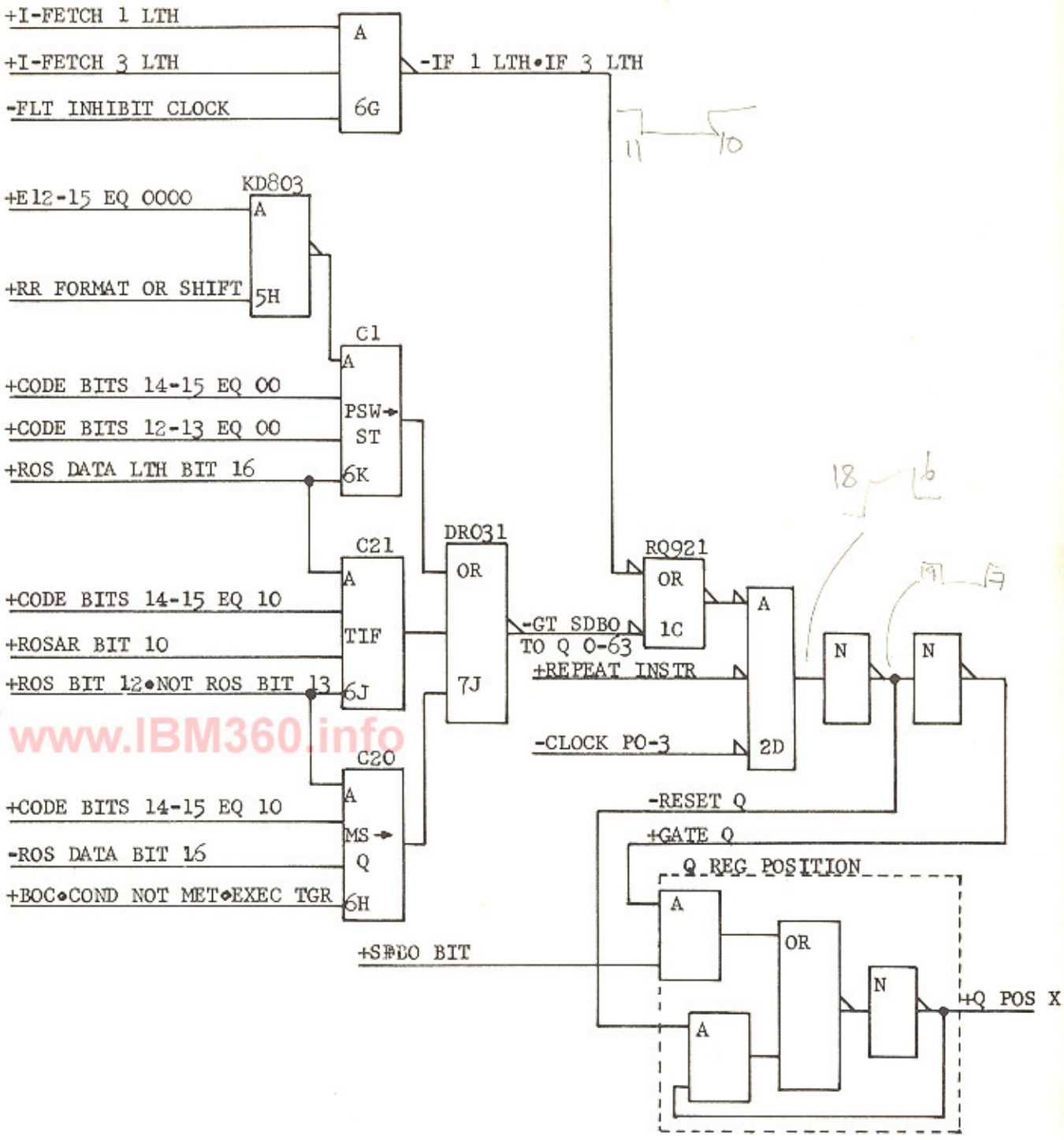

GATING SDBO TO Q REG.

2-10

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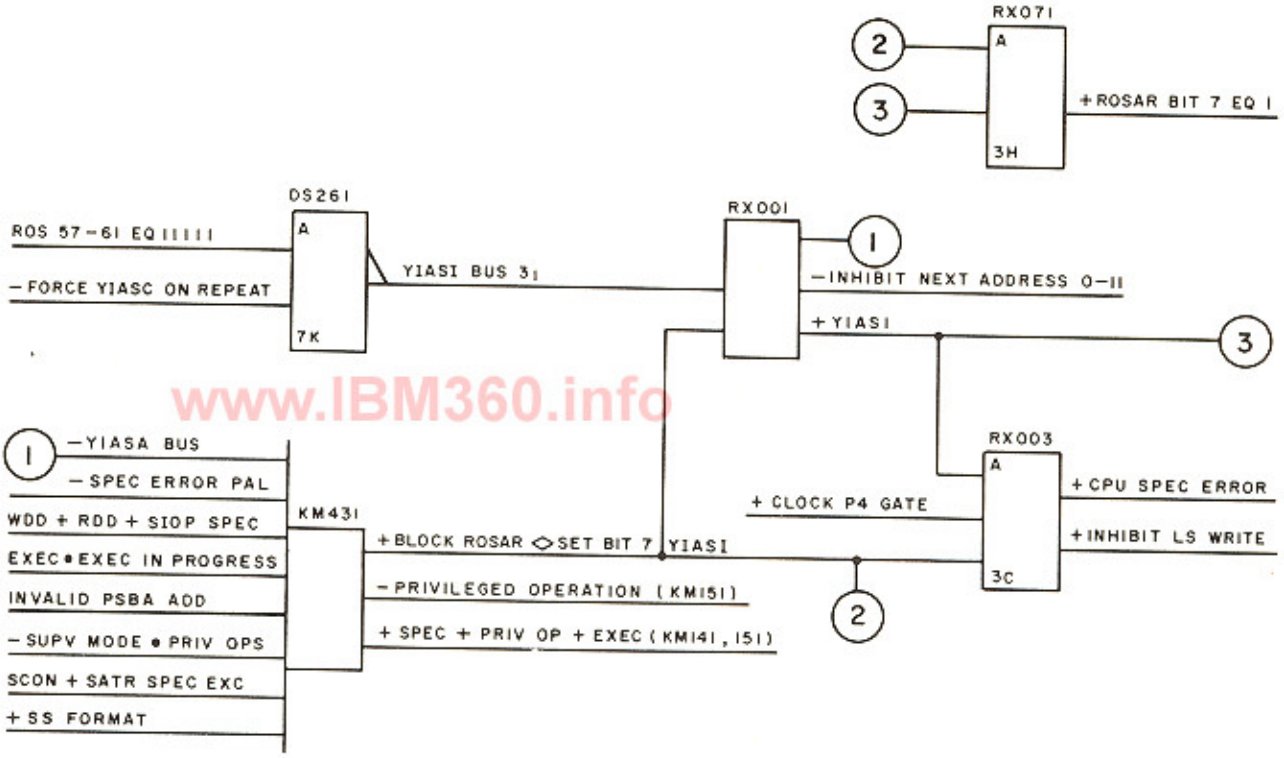

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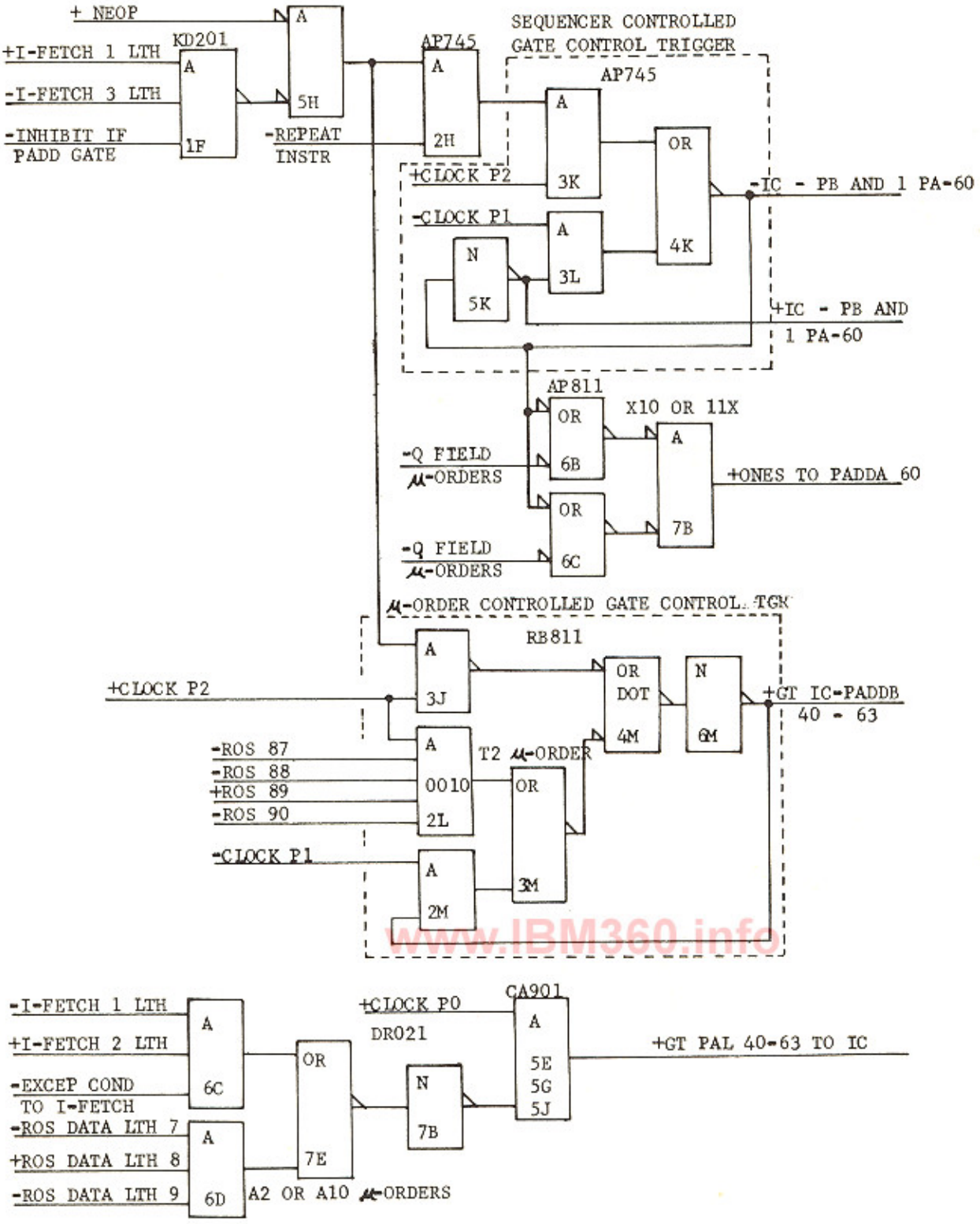
SPEC μ-Order (K31) Force ROS to Ø1Ø

2-12



GATING IC PLUS 8 TO PARALLEL ADDER TO IC.